REMARKS

Claims 1, 3, 4, 6, 7, and 9 are pending, with all claims rejected under 35 U.S.C. 103(a) as being unpatentable over Durham et al. (U.S. Patent No. 5,761,517; hereinafter "Durham") in view of Wang (U.S. Patent No. 5,943,203).

Independent claim 1 has been amended to recite "A frequency regulating circuit ... comprising ... a pulse filter ... configured to suppress at least one clock pulse of said clock signal generated by said clock signal generator, directly in response to said control signal at said control input, such that said control device adjusts said clock frequency instantaneously to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit."

The clock pulse is suppressed directly in response to the control signal such that the control device adjusts the clock frequency instantaneously, and therefore the frequency regulating circuit of independent claim 1 has a fast reaction time. As soon as current consumption exceeds a predefined threshold value, at least one clock pulse is suppressed, and the circuit is basically placed in a hold mode. During the hold mode there is no longer a load. A brief time later the current consumption falls below the threshold value, and the clock pulse suppression is stopped. This process can be repeated again and again depending on the current profile. There is only full frequency mode (i.e., no clock pulse suppression) or hold mode (i.e., clock pulse suppression), and nothing in between (e.g., 3 clock pulses passed, 5 suppressed, 2 passed, 3 suppressed, etc.).

In contrast, Durham's circuit has defined frequency levels, and these levels are not adjusted directly in response to a control signal. Referring to Durham's Figures 1A and 1B, Durham's circuit changes the output of an oscillator clock 27 prior to its input to dynamic logic circuit elements as a system clock signal 20. The oscillator clock signal is controlled based upon a signal generated by a sensor 18 that determines the power consumption of the integrated circuit. The frequency of the clocked signal 20 is reduced/increased incrementally (explained below) based upon the determined level of power consumption. A pattern generator 17 inputs a digital signal to a series of interconnected registers 10, 11, 12, 13 which make up a loadable shift register. The output

of the pattern generator 17 is based upon the input from the sensor 18. The bits shifted through the shift register are ANDed 7 with the oscillator clock signal to control the frequency of the system clock 20. Durham's frequency levels are therefore not adjusted directly in response to a control signal, as required by independent claim 1.

Regarding the incremental reduction/increase of frequency, Durham has defined frequency levels 4, 3, 2, 1, 0. See Durham, Figure. 2. Level 4 represents the speed of the system clock 20 equaling the speed of the oscillator clock 27. Level 3 represents the speed of the system clock 20 being 75% of the speed of the oscillator clock 27, that is 3/4 clock pulses passing. Level 2 represents the speed of the system clock 20 being 50%, that is 2/4 clock pulses passing. Level 1 represents the speed of the system clock 20 being 25%, that is 1/4 clock pulses passing. Level 0 represents no clock pulses passing, that is when the system is turned off. See Durham, Figure 4. This frequency increase/decrease happens incrementally using the shift register shown in Figures 1A and 1B. As illustrated in Figure 4, the frequency levels can not be changed from level 4 to level 1 instantaneously. The frequency level increase/decrease happens gradually, making Durham's reaction time significantly slower than that of the circuit of independent claim 1. Durham therefore does not disclose adjusting the clock frequency instantaneously, as required by independent claim 1.

The Examiner's Answer, page 6, second full paragraph, includes a discussion as to whether or not a sensor is instantaneous. In order to avoid confusion, the Examiner should note that the distinction discussed above is directed to the clock frequency adjustment being instantaneous, as opposed to the sensor activity being instantaneous.

Wang fails to make up for Durham's deficiencies.

Independent claim 1 is therefore patentable over the applied references for at least these reasons.

Since independent claims 4 and 7 include limitations similar to the limitations discussed above with respect to independent claim 1, they are patentable over the applied references for at least the same reasons.

All other claims depend either directly or indirectly from the independent claims, and are therefore patentable over the applied reference for at least the same reasons.

Reconsideration and withdrawal of the prior art rejections are therefore respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

Dated: September 30, 2009

Respectfully submitted,

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